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10/065,762	11/15/2002	Wei-Pin Chen	JCLA8424	9203

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EXAMINER	
NICKERSON, JEFFREY L	
ART UNIT	PAPER NUMBER
2142	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/065,762	CHEN ET AL.	
	Examiner	Art Unit	
	JEFFREY NICKERSON	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Application No. 10/065,762 filed on 15 November 2002. The amendment presented on 19 June 2008, which provides change to claims 1-9 and 14-20, specification, and drawings, is hereby acknowledged. Claims 1-20 have been examined.

Specification

2. The amendment presented on 19 June 2008 which provides change to the specification is noted. All prior objections to the specification are hereby withdrawn.

Drawings

3. The amendment presented on 19 June 2008 which provides replacement drawings is noted. These drawings are accepted and all prior objections to the drawings are hereby withdrawn.

Claim Rejections - 35 USC § 101

4. The amendment presented on 19 June 2008 which provides change to claims 1-8 and 14-20 is noted. All prior rejections under 35 USC 101 are hereby withdrawn.

Response to Arguments

5. Applicant's arguments regarding claims 1-20 have been fully considered but they are not persuasive.

Independent claims 1, 9, and 14

Applicant argues that the combined teachings of Kawauchi (US 5,619,653), Nanba (US 4,665,484), and Fujimoto (US 5,418,913) do not teach several limitation in these claims. Specifically, applicant argues that the combined teachings do not teach: "*the write control unit … used to sequentially output a plurality of free message row addresses according to the plurality of distribution complete flags…".*

The examiner respectfully disagrees. Kawauchi teaches the write control unit used to sequentially output a plurality of free message row addresses (Kawauchi: Figure 3, col 4, lines 3-17). Nanba cures the missing limitation and teaches wherein addresses are determined to be free according to a distribution complete flag (Nanba: col 1, lines 17-65). Nanba utilizes a well known test-and-set operation, which performs the same exact function as applicant's claimed "distribution complete flag". Test and set operations perform in the following manner: A resource acquirer *tests* a lock flag/bit to see if the resource is currently locked. If the lock flag indicates 'unlocked' then the resource isn't locked and the resource acquirer takes control of the resource and *sets* the flag to 'locked' status. If the lock flag indicates 'lock' status then the resource is locked and the resource acquirer will retry the test-and-set operation later. If the resource acquirer obtained control of the resource, then once the resource acquirer is finished with the resource, the acquirer sets the flag to 'unlocked' status. Therefore, when Kawauchi is combined with Nanba, access to the shared message rows (via the buffer controller

returning a pointer to the message row) is obtained by analyzing the lock flag status of each row.

Applicant further argues that the write control unit and read control unit as claimed are different than Kawauchi's single buffer controller.

The examiner respectfully disagrees, as splitting the controller into two is a mere design choice when the single buffer controller performs the same functions as the combined write control unit and read control unit.

Applicant further argues that the following limitation is not taught by the combined teachings: "*after the destination controller reads the message, the distribution flag and write complete flag of the message row are both cleared.*"

The examiner respectfully disagrees for reasons similar to those stated above regarding the combination of Kawauchi and Nanba. Kawauchi teaches that the write complete flag of the message row is cleared after read (Kawauchi: col 5, lines 22-35; col 3, lines 31-56). Nanba teaches using test-and-set operations, which, when applied by the destination controller, will unlock the row upon read completion, i.e. clear the distribution flag.

Therefore, the rejections of these claims are hereby maintained.

Dependent claims 2-8, 10-13, and 15-20

Applicant argues these claims conditionally on the arguments above.

Therefore, the rejections of these claims are hereby maintained.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1, 3, 7-9, 11-14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), and further in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913).

Regarding claim 1, Kawauchi teaches a buffer device (Kawauchi: abstract specifies a data buffer device), for transmitting a plurality of messages between a source and destination, comprising:

a plurality of messages rows (Kawauchi: Figure 3 depicts multiple data columns), for storing the messages that the source intends to transmit to the destination (Kawauchi: abstract), each of the message rows at least comprising a write complete flag (Kawauchi: abstract specifies write attribute flags);

a write control unit (Kawauchi: Figure 3, item 110 depicts the buffer controller), coupled to the source and the plurality of message rows (Kawauchi: Figure 3, see also col 4, lines 3-17), used to sequentially output a plurality of free message row addresses (Kawauchi: Figure 3; col 4, lines 3-17 specifies that the write pointer sequentially acquires buffer addresses), wherein when the message transmitting queue still has a free message row, the source controller reads an address of the message row that is currently free among said plurality of message rows (Kawauchi: Figure 3; col 4, lines 3-17; col 4, lines 45-58 specifies it does not use addresses if they've already been written to), and when the source completes writing the message of the message row that is currently free, the write complete flag of the message row that is currently free is set (Kawauchi: Figure 3, col 4, lines 3-17; col 4, lines 45-58 specifies the write attribute bit is flagged once writing is complete), and when the message transmitting queue has no free message row, said write control unit outputs a non-free message row signal (Kawauchi: Figure 3, item 100; col 3, lines 31-57 specify there is a "reception ready" signal for the buffer device, equivalent to a NOT "not free address" signal and used for the same purpose);

and a read control unit (Kawauchi: Figure 3, item 110 depicts the buffer controller), coupled to the destination and the plurality of message rows (Kawauchi: Figure 3; see also col 3, lines 23-57), to sequentially read the message of the message row when the write complete flag is set, wherein after the destination reads the message, the write complete flag of the message row is cleared (Kawauchi: col 5, lines 22-35).

Kawauchi does not teach the use of a distribution complete flag, retrieving addresses based on the distribution complete flag, setting the distribution flag once the address has been retrieved, and clearing the distribution complete flag. Nor does Kawauchi teach informing the destination when the data is ready to be read.

Nanba, in a similar field of endeavor, teaches the use of a distribution complete flag, retrieving addresses based on the distribution complete flag, setting the distribution flag once the address has been retrieved, and clearing the distribution complete flag. (Nanba: col 1, lines 17-45 specifies a test and set instruction, which uses a lock control flag on shared memory).

Nanba does not teach informing the destination when the data is ready to be read.

Fujimoto, in a similar field of endeavor, teaches informing the destination when the data is ready to be read (Fujimoto: Figure 4, "Receiver's Identity" rows; Figure 6, item 110; col 13, lines 22-46 specifies an interrupt is sent to the processor associated with the queue so it can start reading).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Nanba for using a test and set instruction and the teachings of Fujimoto for sending interrupts to receiving processors. The teachings of Nanba and Fujimoto, when implemented in the Kawauchi system, will allow one of ordinary skill in the art to handle multithreaded writes to shared memory and allow for organized reading from destination controllers by using interrupts. One of

ordinary skill in the art would be motivated to utilize the teachings of Nanba and Fujimoto in the Kawauchi system in order to prevent race conditions during writing to shared memory by multiple threads and allow efficient reading of a queue from multiple processors by using interrupts.

Regarding claim 3, the Kawauchi/Nanba/Fujimoto system teaches wherein the read control unit comprises:

a read pointer control unit, to store a read address of the message transmitting queue (Kawauchi: Figure 3, item 103), wherein when the destination controller completes reading the message of the message row pointed to by the read address, said read pointer control unit clears the distribution complete flag and the write complete flag of the message row (Kawauchi: col 5, lines 22-35; Nanba: col 1, lines 17-45), and progresses the read address (Kawauchi: abstract specifies reading is sequential);

a read buffer, coupled to the read pointer control unit and the plurality of message rows, to temporarily store the message of the message row pointed to by the read address (Fujimoto: Figure 10, items 115 provides the receiving processor is storing the message);

and a read request multiplexer, coupled to the read pointer control unit and the write complete flags of the plurality of message rows, to output the read request according to the write complete flag of the message row pointed to by the read address (Fujimoto: col 1, line 50 – col 2, line 6 specifies that obtaining read pointer address from flag status in a queue is well known in the art).

Regarding claim 7, the Kawauchi/Nanba/Fujimoto system teaches wherein the source is a central processing unit (Fujimoto: Figure 1a, item 1 and Figure 9, items 114).

Regarding claim 8, the Kawauchi/Nanba/Fujimoto system teaches wherein the destination is a central processing unit (Fujimoto: Figure 1a, item 2 and Figure 9, items 114).

Regarding claim 9, this method claim comprises limitations corresponding to that of claim 1 and the same rationale of rejection is used, where applicable. And wherein the rows are referenced with read and write pointers (Kawauchi: Figure 3, item 102; Figure 3, item 103).

Regarding claim 10, the Kawauchi/Nanba/Fujimoto system teaches wherein when the write pointer is progressed and points to a message row whose distribution complete flag is set, a not free message row signal is asserted to inform the source controller.

Regarding claim 11, this method claim comprises limitations corresponding to that of claim 7 and the same rationale of rejection is used, where applicable.

Regarding claim 12, this method claim comprises limitations corresponding to that of claim 8 and the same rationale of rejection is used, where applicable.

Regarding claim 13, the Kawauchi/Nanba/Fujimoto system teaches wherein the read request is an interrupt request of the CPU (Fujimoto: col 13, lines 22-46 specifies an interrupt is sent to the processor associated with the queue so it can start reading).

Regarding claim 14, this message transmitting queue claim comprises limitations corresponding to that of claim 9 and the same rationale of rejection is used, where applicable.

Regarding claim 19, this message transmitting queue claim comprises limitations found in and corresponding to that of claim 9 and the same rationale of rejection is used, where applicable.

8. Claims 2, 10, 16-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), Nanba (US 4,665,484), and Fujimoto (US 5,418,913), and further in view of Fried et al (US 5,142,676).

Regarding claim 2, the Kawauchi/Nanba/Fujimoto system teaches wherein the write control unit comprises:

a write pointer control unit (Kawauchi: Figure 3, item 102), for storing a write address of the message row that is currently free (Kawauchi: col 4, lines 3-17), wherein after the source controller reads the write address of the message row that is currently

free, said write pointer control unit sets the distribution complete flag of the message row that is currently free (Nanba: col 1, lines 17-45 specifies a test and set instruction, which uses a lock control flag on shared memory), and progresses the write address of the message row that is currently free (Kawauchi: col 4, lines 3-17 provide the write addresses are progressed sequentially), and when the source controller completes writing the message of the message row, sets the write complete flag of the message row (Kawauchi: col 4, lines 46-58 specifies changing the write data attribute flag after writing data);

The Kawauchi/Nanba/Fujimoto system does not teach a distribution complete flag multiplexer or a distribution address multiplexer.

Fried, in a similar field of endeavor, teaches:

a distribution complete flag multiplexer (Fried: Figure 2, item 62), coupled to the write pointer control unit (Fried: Figure 3, item 85; col 6, lines 24-39) and the distribution complete flags of the plurality of message rows, (Fried: Figure 2, items 58; col 5, lines 28-33) to output a not-distributed signal (Fried: NOT FOUND signal) according to the distribution complete flag of the message row pointed to by the write address (Fried: col 7, lines 37-63 specifies that if a shared memory row has been already locked, a NOT FOUND signal is used to indicate the row can't be accessed);

and a distribution address multiplexer (Fried: Figure 3, items 102, 104, 106; col 7, lines 20-36), coupled to the distribution complete flag multiplexer and the write pointer control unit, to output the affirmative of the write address and the no free message row signal according to the not-distributed signal (Fried: col 7, lines 20-63 specify that when

it is determined the segment address has not been locked, then the LOCK signal is applied to lock the segment and then the segment is written to; and when it is determined the segment address has been locked the DISALLOW signal is asserted; See also col 6, lines 24-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Fried for managing locked memory segments with NOT FOUND and DISALLOW signals. The teachings of Fried, when implemented in the Kawauchi/Nanba/Fujimoto system, will allow one of ordinary skill in the art to identify memory segments of the queue between two processors that have been locked and disallow writing to locked segments while allowing locking and writing to unlocked segments. One of ordinary skill in the art would be motivated to utilize the teachings of Fried in the Kawauchi/Nanba/Fujimoto system in order to allow multiple processors to identify which memory segments are currently locked and which are available for locking and writing.

Regarding claim 10, this claim contains limitations found within and corresponding to claim 2 and the same rationale of rejection is applied, where applicable.

Regarding claim 16, this claim contains limitations found within and corresponding to claim 2 and the same rationale of rejection is applied, where applicable.

Regarding claim 17, this claim contains limitations found within and corresponding to claims 1 and 2 and the same rationale of rejection is applied, where applicable.

Regarding claim 18, the Kawauchi/Nanba/Fujimoto/Fried system teaches wherein when the source controller receives the no free message row signal, a request is issued to ask for the free message row from the message transmitting queue every predetermined period (Fried: col 3, line 64 – col 4, line 20 specifies if the requesting processor cannot access the memory address it will repeat is request after a certain amount of time).

Regarding claim 20, the Kawauchi/Nanba/Fujimoto/Fried system teaches wherein when the source controller receives a free message row address, a firmware records said free message row address till an associated message has been written to the free message row address completely (Fried: Figure 1, item 24 depicts the locked address memory table; col 3, lines 40-56 specify a table maintains locked memory addresses and the corresponding processor ID that locked them).

9. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), Nanba (US 4,665,484), and Fujimoto (US 5,418,913), and further in view of Balmer et al (US 5,724,599).

Regarding claim 4, the Kawauchi/Nanba/Fujimoto system teaches wherein each message row comprises data the source intends to transmit to the destination (Kawauchi: abstract).

The Kawauchi/Nanba/Fujimoto system does not teach wherein the data is a command row and a data row.

Balmer, in a similar field of endeavor, teaches wherein the data can be an command (instruction) row and a data row (Balmer: Figure 2, items 11, 12, 13, 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Balmer for splitting data into instruction rows and data rows. The teachings of Balmer, when implemented in the Kawauchi/Nanba/Fujimoto system, will allow one of ordinary skill in the art to organize data sending from one processor to the next by splitting it into instructions and data. One of ordinary skill in the art would be motivated to utilize the teachings of Balmer in the Kawauchi/Nanba/Fujimoto system in order to allow the receiving processor to easily identify which part of the message is an instruction and which part is data.

Regarding claim 5, the Kawauchi/Nanba/Fujimoto/Balmer system teaches wherein the size of the command row is four bytes (Balmer: col 10, line 52 – col 11, line 10 specify 32 bit instructions).

Regarding claim 6, the Kawauchi/Nanba/Fujimoto/Balmer system teaches wherein the size of the data row is a multiple of four bytes (Balmer: col 10, line 52 – col 11, line 10 specify data is stored in 32 bit words).

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), Nanba (US 4,665,484), and Fujimoto (US 5,418,913), and further in view of IEEE ("1003.1 Standard for Information Technology – POSIX"; Base definitions, Issue 6; 6 December 2001).

Regarding claim 15, the Kawauchi/Nanba/Fujimoto system does not teach wherein the length of a message exceeds the atomic read/write size that can be processed by said controllers.

IEEE, in a similar field of endeavor, teaches wherein the length of a message exceeds the atomic read/write size that can be processed by said controllers (IEEE: pg 251, definition for {PIPE_BUF} provides that handling non-atomic writes due to excessive file size can be handled by any POSIX compatible OS, they just won't be atomic).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of IEEE for using atomic read/write operations under a certain size limit. The teachings of IEEE, when implemented in the Kawauchi/Nanba/Fujimoto system, will allow one of ordinary skill in the art to write messages over a certain size non-atomically. One of ordinary skill in the art would be

motivated to utilize the teachings of IEEE in the Kawauchi/Nanba/Fujimoto system in order to comply with computing standards.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY NICKERSON whose telephone number is (571)270-3631. The examiner can normally be reached on M-Th, 8:30-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571-272-3868. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. N./
Jeffrey Nickerson
Examiner, Art Unit 2142

/Andrew Caldwell/
Supervisory Patent Examiner, Art Unit 2142